CLAIMS

What is claimed:

1. A method of making a semiconductor transistor, comprising:

locating a substrate of a doped semiconductor material in a chamber;

introducing a gas into the chamber;

repeatedly increasing and decreasing a plasma generating voltage potential across the gas in the chamber between a cathode and an anode while the substrate is in the chamber, a transient ion plasma generating from the gas after an increase in magnitude of the plasma generating voltage potential and degenerating after a decrease in magnitude of the plasma generating voltage potential;

repeatedly increasing and decreasing an implantation voltage potential between the ion plasma and the substrate, ions of the plasma accelerating towards and implanting into a gate dielectric layer formed on the substrate after an increase in magnitude of the implantation voltage potential; and

forming a conductive transistor gate on the dielectric layer implanted with the ions.

2. The method of claim 1 wherein the gas includes nitrogen.

3. The method of claim 2 wherein the ions include nitrogen ions.

4. The method of claim 1 wherein the plasma generating voltage is generated by repeatedly increasing a voltage of the cathode to a positive voltage and decreasing the voltage of the cathode.

5. The method of claim 1 wherein the plasma generating voltage has a magnitude of at least 1 kV.

6. The method of claim 1 wherein subsequent increases in the plasma generating voltage are spaced by less than 1 second.

7. The method of claim 1 wherein the plasma generating voltage is less than 50% of its maximum for at least 95% of the time.

8. The method of claim 1 wherein the ion plasma generates in an area in the chamber between the anode and the substrate.

9. The method of claim 1 wherein the implantation voltage potential has a maximum voltage potential that has a maximum magnitude of less than 80 V.

10. The method of claim 9 wherein the implantation voltage potential has a

maximum magnitude of more than 10V.

11. The method of claim 1 wherein the implantation voltage potential has a magnitude of less than 4% of a maximum magnitude of the plasma generating voltage.

12. The method of claim 1 wherein a period of the implantation voltage potential is substantially the same as a period of the plasma generating voltage potential.

13. The method of claim 1 wherein the plasma generating voltage potential is generated by applying a voltage having a positive maximum to the cathode and the implantation voltage potential is created by applying a voltage having a negative maximum to the substrate.

14. The method of claim 1 wherein the ions increase a dielectric constant of the gate dielectric layer.

15. The method of claim 1 further comprising:

adjusting a magnitude of the implantation voltage potential.

16. A method of making a semiconductor transistor, comprising:

locating a substrate of a doped semiconductor material in a chamber;

introducing a gas into the chamber;

repeatedly increasing a voltage on a cathode to a positive value and decreasing the voltage on the cathode so as to repeatedly increase and decrease a plasma generating voltage potential across the gas in the chamber between the cathode and an anode while the substrate is in the chamber, an ion plasma generating from the gas after an increase in magnitude of the plasma generating voltage potential and degenerating after a decrease in magnitude of the plasma generating voltage potential;

repeatedly decreasing a voltage on the substrate to a negative value and increasing the voltage on the substrate so as to repeatedly decrease and increase an implantation voltage potential between the ion plasma and the substrate, ions of the plasma accelerating towards and implanting into a gate dielectric layer formed on the substrate after a decrease of the implantation voltage potential; and

forming a conductive transistor gate on the dielectric layer implanted with the ions.

17. The method of claim 16 wherein the implantation voltage potential has a maximum magnitude of more than 10V but less than 20V.

18. The method of claim 16 wherein a period of the implantation voltage potential is substantially the same as a period of the plasma generating voltage potential.

19. The method of claim 16 wherein the ions increase a dielectric constant of the gate dielectric layer.

20. A method of making a semiconductor transistor, comprising:

locating a substrate of a doped semiconductor material in a chamber;

introducing a gas into the chamber;

repeatedly

(i) (a) increasing a plasma generating voltage potential across the gas in the chamber between a cathode and an anode while the substrate is in the chamber, a transient ion plasma generating from the gas after an increase in magnitude of the plasma generating voltage potential, and (b) decreasing an implantation voltage potential between the ion plasma and the substrate, the ions accelerating towards and implanting into a gate dielectric layer formed on the substrate after an increase in magnitude of the implantation voltage potential

and

(ii) (a) decreasing the plasma generating voltage potential, the plasma degenerating after a decrease in magnitude of the plasma generating voltage potential, and (b) increasing the implantation voltage potential, whereafter fewer ions implant into the gate dielectric layer; and

forming a conductive transistor gate on the dielectric layer implanted with the ions.

21. The method of claim 20 wherein subsequent increases in the plasma generating voltage are spaced by less than 1 second.

22. The method of claim 20 wherein the plasma generating voltage is less than 50% of its maximum for at least 95% of the time.